H-737 Version 2.0

Logical Address Assignment for SELEX

Jürgen Engelfried

May 20, 1996

Abstract

In this document we like to collect all information concerning the cable plan and the assignements of the logical addresses to frontend modules. This is relevant for the DAQ system, the *unpacker* used by offline and online software as well as for the offline analysis code itself.

1 Introduction

We have more than 600 frontend modules in SELEX. Most of the modules (with exception of RMH) have a place to put a logical address either in the module header (for Fastbus) or in the data word itself (CROS), where these bits are otherwise unused. We propose here to use these bits as a detector identification, which will make the unpacker independent of the physical location of the frontend modules.

In a later version of this document we will also include the detailed cable plan for each detector.

The unpacker can than unpack the data according to the needs of every detector, which should simplify later processing of the data, and has not to put the data in an generic common block for the frontend module used.

2 ADCs

The detectors using the 1881 Fastbus ADCs (64 channels per module) are:

Photon 1: 620 blocks or 10 modules

Photon 2: 726 blocks or 12 modules

Photon 3: 328 blocks or 6 modules

NCAL: 50 scintillators or 1 module

RICH: some channels in 1 module

Since we have 16 bits available, we propose the following assignment, which will also give us access to the geographical address (not provided automatically with this header option):

Bits	31 28	27 24	23 22	21 16
	Detector Id	Module #		geographical Address

Table 1: ADC Header

Detector	Detector Id	Module #
Photon 1	1	1 – 10
Photon 2	2	1 – 12
Photon 3	3	1 – 6
NCal	4	1
RICH	5	1

Table 2: Detector IDs for ADCs

3 TDCs

The 10C6 TDC (32 channels/module) serve for two types of detectors: The "Brasilien" chambers and the "Iowa" chambers.

We have 9 Brasilien chambers (3 chambers in each Vee stand); they are vector chambers with a fine grid of 10 cells of eight wires each in the center and a coarse grid of 15 cells of 6 wires on both sides. For the fine cells one preamp card serves 16 channels of two neighbouring cells, and the cables are running over 32 channel repeater modules to the TDCs. For the coarse cells one preamp board serves the 12 wires of 2 neighbouring cells, (4 channels of each preamp board are unsused), and the cables are running over repeater boards to the TDCs, were we will swicth off unsused channels. We need for each chamber 11 TDC modules, 4 for each coarse region and $2\frac{1}{2}$ for the fine region. For the cabling plan I am following a note of Lev Uvarov, dated May 10, 1996.

We have 2 Iowa chambers, which consist of 2 staggered planes each. 11 cables from 11 preamps are running to $5\frac{1}{2}$ TDC modules and will be connected in order.

We will use 5 TDC crates, 4 of them filled with 22 TDCs to readout 2 Brasilien chambers each, and one with 23 TDCs to readout 1 Brasilien and the 2 Iowa chambers. (This has to be check for head load, but does not influence the logical address).

We have 8 bits available to assign the detector Ids.

Bits	31 28	27 24
	Chamber #	Module #

Table 3: TDC Header

Detector	Chamber #	Module #
M1 Spectro, X1	1	1 – 6
M1 Spectro, X2	2	1 – 6
VeeA, U	5	1 – 11
VeeA, Y	6	1 – 11
VeeA, X	7	1 – 11
VeeB, V	8	1 – 11
VeeB, Y	9	1 – 11
VeeB, X	10	1 – 11
VeeC, U	11	1 – 11
VeeC, Y	12	1 – 11
VeeC, X	13	1 – 11

Table 4: Chamber IDs and Module Numbers for TDCs

4 CROS

The CROS system serves for several detectors with in total about 10000 channels. One RML has 32 channel, and only 7 bits of the 16 bit word are used (2 as id, 5 for the channel number). We can use 9 bits for the logical address.

The detectors connected to CROS are:

PWCs: 5-16 RMLs/plane, 14 planes total

TRD: 8 RMLs/plane, 6 planes total

RICH: 2848 channels in 89 RMLs

NCAL: $1\frac{1}{2}$ RMLs/plane, 14 planes total

BTRD: 1 RML

We propose the following assignment and interpretations for the detectors. In this scheme we need some special decoding for the NCAL, but we anyway expect only a small number of hits there:

5 FSDA

We have 44 Silicon planes in the experiment, and we have 8 bits in the FSDA header available for a logical address. A FSDA reading out in the "non-merging" mode will produce 2 headers. The following detectors are read out by the FSDA:

Beam: 8 planes

Vertex: 8 planes

Mosaic: 12 planes

Quad: 8 planes

LASD, double sided: 12 planes (6 at 2 locations)

LASD, single sided: 6 planes

Pixel: not yet known

Bits	15 14	13 12	1110	9	8 6	5	4 0
Data Word	0	logical address					channel
Assignment		plane id			Module #		channel
PWC		plane id			wire number		
BTRD		plane id			wire number		
TRD		plane id			wire number		
RICH			Phototube number				
NCAL				ncal plane		wire number	

Table 5: CROS Data word and interpretation for different detectors

Detector	Plane Id	Module #
DPWC X1	1	0 – 8
DPWC Y1	2	0 – 5
DPWC X2	3	0 – 9
DPWC Y2	4	0 – 5
DPWC U3	5	0 – 8
DPWC V3	6	0 – 8
DPWC Y4	7	0 – 9
DPWC X4	8	0 – 15
DPWC V5	9	0 – 9
DPWC U5	10	0 – 15
DPWC Y6	11	0 – 9
DPWC X6	12	0 – 15
DPWC Y7	13	0 – 9
DPWC X7	14	0 – 15
BTRD	16	1
TRD X1	17	0 – 7
TRD X2	18	0 – 7
TRD X3	19	0 – 7
TRD X4	20	0 – 7
TRD X5	21	0 – 7
TRD X6	22	0 – 7
RICH	24 – 29	0 – 15
NCAL	15,31	0 – 15
Spare	0,23	

Table 6: Plane Ids for CROS

Bits	31 28	27 24
	Detector #	Module #

Table 7: FSDA Header

Detector	Detector #	Module #
Beam	1	1 – 8
Vertex	2	1 – 8
Mosaic	3	1 – 8
Quad	4	1 – 12
LASD, double, n	5	1 – 6
LASD, double, p	6	1 – 6
LASD, single	7	1 – 6
Pixel	8	

Table 8: Detector and Module numbers for FSDAs