H-728

Proposal For E781 Raw Data Format

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Abstract

This document contains a proposal for the raw data format for SELEX.

1 General Structure

We present a few tables to describe a proposed raw data format. The general concept is to subdivide the event record into blocks. These blocks contain either raw data, or possible calculated quantities about the event; also Monte Carlo blocks are possible. The first word of each block contains a block id in bits 24-31, and an inclusive byte count in bits 0-23. The scheme is shown pictorially in table 1.

The very first word of the event record is the inclusive byte count for the entire record.

The first block (block id 0) is the event header. It contains some important event decriptors in fixed positions at the beginning of the event record. This block can grow in length arbitrarily, but new information can only be appended. In addition to run number, spill number, etc, we have included two pointers to "directories". One directory (block id 1) contains pointers to the raw data coming from the various readout controllers. The other directory (block id 2) contains pointers to blocks from other sources such as filter information, Monte Carlo, etc. This format will facilitate the partial unpacking of the event record and also makes the unpacking independent of the stream assignment of the readout controllers, which will be optimized to balance the amount of data per stream.

Block ids 3-31 are reserved for raw data streams. Each stream contains data from one or more readout controllers. The general format for these subblocks is briefly described in the next section. More detailed descriptions of the data format from the individual frontend modules can be found in H643.

Further block id assignments will be allocated as needed.

2 Readout Controller Headers

Every readout controller (FSCC, DYC+, CROS, RMH, SCC) will produce a 2 word header associated with the data read out. The first word contains the length of the transmitted data in some unit and a 4 bit event number which will assure synchronization. The second word contains a readout controller id and for the FSCC the spill number, otherwise 0.

These readout controller ids will be assigned once and forever to facilitate later unpacking of the event. Table 2 contains the assignments.

Bits	31 24	23 16	15 12	11 0	
	Event Length				Inclusive Byte Count
	0	Eventheader Length			Inclusive Byte Count
	Run Number				increasing from 10000
	Spill Number in Run				Reset at begin of run
	Event Number in Run				Reset at begin of run
	Event Number in Spill				Reset at begin of spill
	Trigger Mask				
	Version Number				
	Pointer to Readout Controller Pointer Block				
	Pointer to Blocks Pointer Block				
	. .				
	1	Length			Readout Controller Pointer Block
	Pointer to SCC 1				
	Pointer to SCC 2				
	Pointer to FSDA 1				
	Pointer to FSDA 2				
	Pointer to ADC 1				
	Pointer to ADC 2				
	Pointer to TDC 1				
	Pointer to TDC 2				
	Pointer to TDC 3				
	Pointer to TDC 4				
	Pointer to TDC 5				
	Pointer to TDC 6				
	Pointer to TDC 7				
	Pointer to CROS 1				
	Pointer to CROS 2				
	Pointer to RMH 1				
	Pointer to RMH 2				
	2	Length			Block Pointer Block
	Pointer to Filter Data				
	. .				
	Stream Id	Length			Block Header for Streams (id=3,..,31)
			Evt#	Length	FSCC or DYC+ Header
	Readout Controller Id		Spill Number		Spill number only from FSCCs
	Data from this Readout Controller				See individual tables
	. .				
			Evt#	Length	FSCC or DYC+ Header
	Readout Controller Id		Spill Number		Spill number only from FSCCs
	Data from this Readout Controller				See individual tables
	. .				
	. .				
	Stream Id	Length			Block Header for Streams (id=3,..,31)
	. .				

Table 1: Event Format

Detector	Crate	Readout Controller	Identification	Readout Planes
Misc.	CAMAC	SCC/DYC+	0x5301	Scalers and Latches
	CAMAC	SCC/DYC+	0x5302	Scalers and Latches
Silicon	FSDA 1	FSCC	0x4601	
	FSDA 2	FSCC	0x4602	
Photon	ADC 1	FSCC	0x4101	Photon 1,2
	ADC 2	FSCC	0x4102	Photon 3,4
Drift Chambers	TDC 1	FSCC	0x5401	
	TDC 2	FSCC	0x5402	
	TDC 3	FSCC	0x5403	
	TDC 4	FSCC	0x5404	
	TDC 5	FSCC	0x5405	
	TDC 6	FSCC	0x5406	
	TDC 7	FSCC	0x5407	
	TDC 8	FSCC	0x5408	
TRD, RICH	CROS	CSB.V/DYC+	0x4301	TRD, RICH
DPWC	CROS	CSB.V/DYC+	0x4302	DPWC
LPWC	RMH	RMH/DYC+	0x5201	
	RMH	RMH/DYC+	0x5202	

Table 2: Assigned Identification for each Readout Controller